

100Gbase LR4 1310nm Single-Mode 10km SFP Transceiver BT-QSFP28-S10-100G



Features

- Up to 10km transmission distance
- Supports 103.1Gb/s aggregate bit rate
- 4x26Gb/s cooled LAN-WDM DFB TOSA
- 4x26Gb/s PIN ROSA
- Single +3.3V power supply
- Power consumption $\leq 3.5W$
- Operating case temperature: 0~70°C

Applications

- 100GBASE-LR4 Ethernet Links

Compliance

- Compliant with FCC 47 CFR Part 15, Class B
- Compliant to IEEE 802.3ba 100GBASE-LR4
- Compliant with QSFP+ MSA.
- Compliant with SFF-8636.
- Compliant with IEEE802.3bm CAUI-4

Description



100G LR4 10km Transceiver is a high performance, cost effective module for serial optical data communication applications to 100 Gigabit Ethernet links on up to 10km of single mode fiber. QSFP-100G-LR4 is compliant with the QSFP28 MSA, IEEE 802.3ba 100GBASE-LR4 and IEEE 802.3bm CAUI-4. Digital diagnostic functions are available via the I2C management interface, as specified by the QSFP28 MSA. The transceiver is RoHS-6 compliant per Directive 2011/65/EU.

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Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	TSTG	-40		85	°C	
Operating Relative Humidity	RH	5		85	%	
Supply Voltage	VCC	-0.5		3.6	V	
Optical Input Power	PIN	5.5			dBm	
Case Operating Temperature	Top	-5		75	°C	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Case temperature	Tcase	0		70	°C	
Supply Voltage	VCC	3.135	3.3	3.465	V	
Module Power Dissipation	P			3.5	W	
Total Data Rate				103.125	Gbps	
Data Rate, each lane				25.78125	Gbps	
Transmission Distance				10	km	

Optical, Electrical Characteristic

Parameter	Symbol	Min	Typical	Max	Units	Notes
Center Wavelength	CH0	λ_{c1}	1294.53		1296.59	nm
	CH1	λ_{c2}	1299.02		1301.09	nm
	CH2	λ_{c3}	1303.54		1305.63	nm
	CH3	λ_{c4}	1308.09		1310.19	nm
Total Average Launch Power	Ptotal			10.5	dBm	
Average Launch Power per Lane	Peach	-4.3		4.5	dBm	
Optical modulation amplitude per lane	POMA	-1.3		4.5	dBm	
Difference in Launch power between any two lanes(OMA)				5	dB	
Transmitter and Dispersion Penalty per Lane	TDP			3	dB	
Side-Mode Suppression Ratio	SMSR	30			dB	
Extinction Ratio	ER	4			dB	
Transmitter reflectance				-12	dB	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}			IEEE 802.3ba		UI	

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	CH1	λ_{c2}	1299.02		1301.09	nm	
	CH2	λ_{c3}	1303.54		1305.63	nm	
	CH3	λ_{c4}	1308.09		1310.19	nm	
Receiver power(OMA) per lane		Rovl			4.5	dBm	
Difference in receive power between any two lanes(OMA)					4.5	dB	
Receiver sensitivity (OMA), each lane (max)		SENeach			-8.6	dBm	
Receiver reflectance					-26	dBm	
LOSS assert		LOSA	-25		-12	dB/Hz	
LOSS de-assert		LOSD			-11	dB	
LOS Hysteresis				1.5		dB	

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential data input swing per lane	Vin-pp			900	mV	
Differential termination mismatch				10	%	
Eye width			0.46		UI	
Eye height			95		mV	

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential data output swing	Vout-pp	600		1200	mVpp	Note1
		400		800	mVpp	
		300		600	mVpp	
		100		400	mVpp	
Eye width		0.57			UI	
Vertical eye closure	VEC			5.5	dB	
Differential termination mismatch				10	%	
Transition time, 20% to 80%	Tr Tf	12			ps	

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Pin Description

Pin	Name	Description	Notes
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	
20	GND	Ground	
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	+3.3V Power supply transmitter	
30	Vcc1	+3.3V Power supply	
31	LPMODE	Low Power Mode	

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32	GND	Ground	
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	

Recommended Interface Circuit

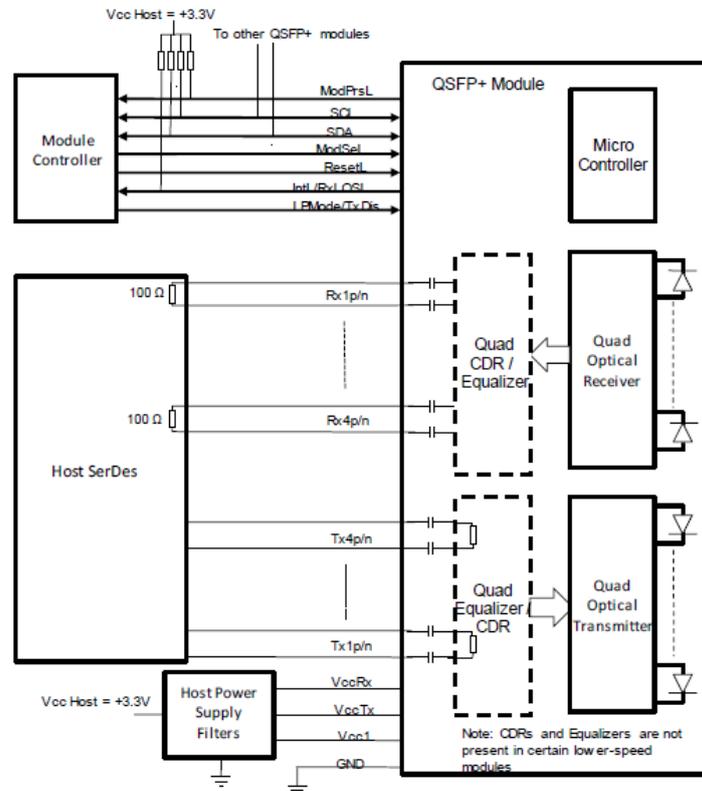


Figure 2 Recommended Interface Circuit

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Digital Diagnostic Memory Map

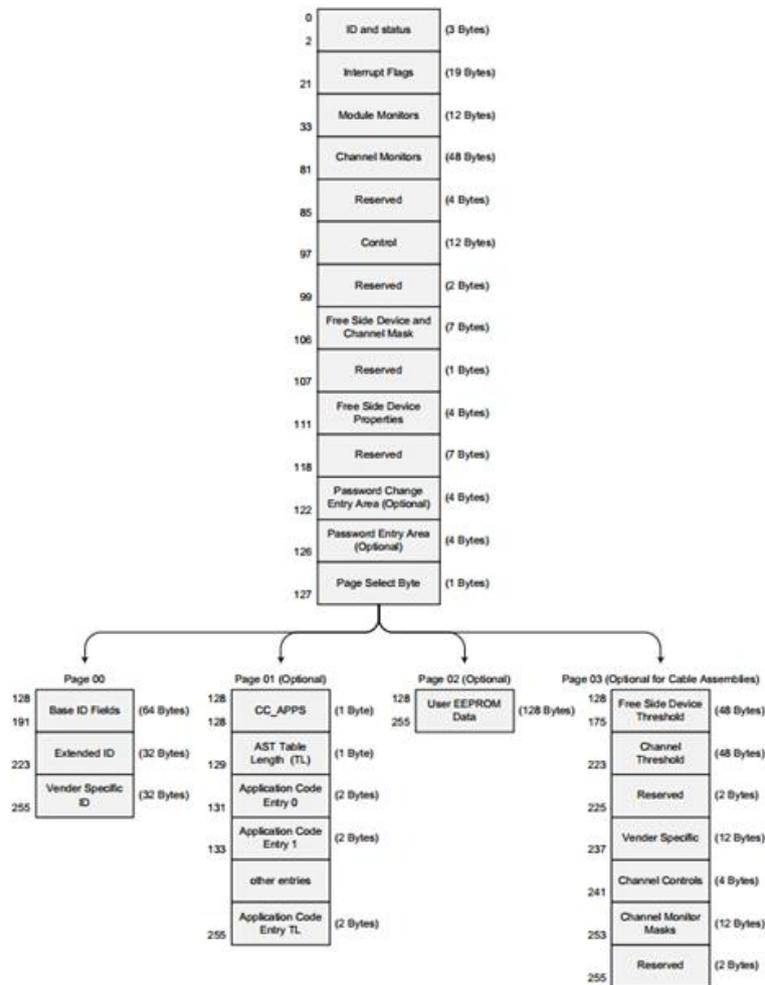


Figure 3 Memory Map